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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
BLACKMAN, ANTHONY J	
ART UNIT	**PAPER NUMBER**
2676	

DATE MAILED: 03/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/828,474	KINJO, NAOTO	
	Examiner	Art Unit	
	ANTHONY J BLACKMAN	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 27-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 27-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Examiner acknowledges the claim for foreign priority and confirms that the certified copies of the priority documents submitted on July 23, 2001, have been received, as requested, in the amendment filed March 23, 2004.

Response to Arguments

2. Applicant's arguments with respect to claims 1-13 and 27-34 have been considered but are moot in view of the new ground(s) of rejection. TANIMOTO et al, US Patent No. 4,622,632 anticipates claims 1-6, 9-11, 31 and 34. NORTON et al, US Patent No. 5,488,713 provides support for TANIMOTO et al with claims 7-8, 13 and 32. BUYTAERT et al, US Patent no. 6,041,135 provides support for TANIMOTO et al with claims 12, 27-30 and 33.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-6, 9-11, 31 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by TANIMOTO et al, US Patent No. 4,622,632.

4. As per claim 1, examiner interprets TANIMOTO et al to meet claim limitations and features as claimed;

an image at a higher drawing level is formed from a computer graphics image formed by computer graphics (column 33, lines 43-56 discloses variable operations of each of a set of processors identify particular pattern (inherently derived from computer graphics) input signals, including various types of edge detection derived from computer displays (column 6, lines 29-33),

said method comprising the steps of:

selecting a particular drawing level from a plurality of drawing levels set in advance for a computer graphics algorithm based on (at least the following underlined feature) at least one of an amount of computation processing, an amount of data and a display resolution (column 33, lines 51-56 teaches processing of a pyramid data structure with a plurality of processors, with each processor associated with each resolution level of the pyramid – column 33, lines 51-56 and figure 2(103) shows the pyramid processing unit);

and performing processing by said computer graphics algorithm at a higher drawing level than said particular drawing level which was selected from said plurality of drawing levels based on (at least the underlined and second conditional feature) editing data in the process of forming said computer graphics image at said particular drawing level or

based on said editing data and attached data thereby forming image data at said higher drawing level (column 33, lines 51-56).

5. As per claim 2, TANIMOTO et al meet limitations of claim 1, including,

wherein said image at the higher drawing level is an image (at least the underlined feature is disclosed) to be printed or an image to be displayed (the following elements of figure 2, Host CPU and Peripheral Devices provide both input and output to the pyramid processor unit figure 2(element –103) and column 5, line 64-column 6, line 5 and 16-34),

and said image data at the higher drawing level is (at least the underlined feature is disclosed) print image data or display image data (the following elements of figure 2, Host CPU and Peripheral Devices provide both input and output to the pyramid processor unit figure 2(element –103) and column 5, line 64-column 6, line 5 and 16-34).

6. As per claim 3, TANIMOTO et al meet limitations of claim 1, including,

wherein said image at the higher drawing level is an output,

said image data at the higher drawing level is output image data, and said processing by said computer graphics algorithm at the higher drawing level (the drawing levels are represented by the pyramidal resolution levels) is performed in a process of outputting image (following the cites above in claim 3 regarding the display image data, it is inherent that the Peripheral devices and Host CPU fully disclose the following limitations

of claim 4 as claimed - Host CPU and Peripheral Devices provide both input and output to the pyramid processor unit figure 2(element –103) and column 5, line 64-column 6, line 5 and 16-34).

7. As per claim 4, TANIMOTO et al meet limitations of claim 1, wherein when said computer graphics image is formed, said particular drawing level is selected from said plurality of drawing levels for (the second conditional underlined feature is taught) feature each image component in an imaged scene or for each processing operation performed for producing a specified particular effect on said computer graphics image (column 33, lines 51-56 with the specified particular effects represented by the local and global transformations on selected data elements at different levels of resolution).

8. As per claim 5, TANIMOTO et al meet limitations of claim 1, including, wherein a plurality of computer graphics algorithms are further prepared (the algorithms are represented by the processors – may be variably processed with at least pattern means -column 33, lines 43-55),

and a particular algorithm is selected from said plurality of computer graphics algorithms based on at least (the at least third and underlined conditional feature is taught) one of said amount of computation processing, said amount of data and said display resolution (column 33, lines 51-56 teaches processing of a pyramid data structure with a plurality of processors, with each processor associated with each resolution level of the pyramid – column 33, lines 51-56 and figure 2(103) shows the pyramid processing unit),

and for the thus selected particular algorithm, said particular drawing level is selected from said plurality of drawing levels (drawing levels are represented by resolution levels - column 33, lines 43-55).

9. As per claim 6, TANIMPOTO et al meet limitations of claim 5, including, wherein when said computer graphics image is formed, said particular algorithm is selected from said plurality of computer graphics algorithms (the at least second and underlined conditional feature is taught) for each image component in an imaged scene or for each processing operation performed for producing a specified particular effect on said computer graphics image (column 33, lines 51-56 – the processors executed simultaneously on local and global transformations on selected data elements represent the particular effects as claimed).

10. As per claim 9, TANIMOTO et al meet limitations of claim 1, including, wherein the process of forming the computer graphics image at the particular drawing level is performed in an image processor and the processing by said computer graphics algorithm at the higher drawing level is performed in the same image processor (column 33, lines 51-56 and figure 2 (element 103) shows the pyramidal processing unit that contains a plurality of processors (one processor for each resolution level of figure 1 beginning with the lower level processor at "0" and increasing to the higher level processor at "7" comprise the pyramidal processing unit).

11. As per claim 10, TANIMOTO et al meet limitations of claim 9, including, wherein said image processor is a Personal Computer (the pyramidal processing unit (figure 2, element 103) is representative of the Personal Computer).

12. As per claim 11, TANIMOTO et al, meet limitations of claim 1, including, wherein processing operations at different drawing levels including the process of forming the computer graphics image at the particular drawing level (column 6, lines 21-25 discloses the transfer of array data between the pyramid processing unit and the host processor)
and the processing by said computer graphics algorithm at the higher drawing level are performed by sharing among a plurality of image processors interconnected through a communication network (column 6, lines 21-25 discloses the transfer of array data between the pyramid processing unit and the host processor – the pyramid processor a plurality of processors with each processor associated with one of the levels of "0" to "7" of figure 1).

13. As per claim 31, TANIMOTO et al meet limitations of claim 1, including, wherein the selecting of a drawing level is based on a display resolution (column 33, lines 51-56 discloses levels of resolution among the different levels of the pyramid processing unit and figure 2(103) shows the pyramid processing unit).

14. As per claim 34, TANIMOTO et al meet limitations of claim 1, including, wherein an image processing software for the computer graphics image is based on performance of a CPU of a personal computer forming the computer graphics image (see column 6, lines 21-25 discusses transfer of the array data to the pyramid processor (represents the image processing software) from the host computer (represents the CPU of a personal computer).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 7-8, 13 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over TANIMOTO et al, US Patent No. 4,622,632 in view of NORTON et al, US Patent No. 5,488,713.

17. As per claim 7, TANIMOTO et al meet limitations of claim 1, however, does not explicitly teach, wherein the process of forming the computer graphics image at the particular drawing level is performed in a first image processor, whereas the processing by said computer graphics algorithm at the higher drawing level is performed with a different timing in a second image processor different from said first image processor,

specifically, although TANIMOTO et al disclose a Host CPU and pyramid processing unit containing plurality of processors, there is no teaching regarding different timing between the first processor and second processor (the host processor of claim 8). Conversely, NORTON et al suggest wherein the process of forming the computer graphics image at the particular drawing level is performed in a first image processor, whereas the processing by said computer graphics algorithm at the higher drawing level is performed with a different timing in a second image processor different from said first image processor (figure 3 discloses different speeds between the processors as claimed for symmetric multiprocessors (SMDs) (column 1, lines 64-67) associated with a host uniprocessor workstation- column 1, lines 10-15. It would have been obvious to one skilled in the art at the time of the invention to use the symmetric multiprocessors (SMDs) (column 1, lines 64-67) associated with a host uniprocessor workstation- column 1, lines 10-15 for prediction of parallel processing times between SMDs and a host single processor workstation (column 1, lines 48-55) of NORTON et al to modify a pyramidal processing system facilitating parallel processing of a plurality of resolution levels to execute local and global o f TANIMOTO et al because both inventions are related to similar technology associated with multiprocessors and a host processor to improve the parallel processing operations of TANIMOTO et al by providing accurate predictions of parallel processing times for accurate prediction of parallel processing times (column 1 of NORTON et al , lines 48-55).

18. As per claim 8, TANIMOTO et al as modified by NORTON et al meet limitations of claim 7. Further, TANIMOTO et al disclose a Host CPU associated with a "ring network or other communication means" (column 6, lines 6-10) and figure 2(element 101)-the pyramid processing system represents a personal computer as claimed, wherein said first image processor is a personal computer and said second image processor is a host computer connected to the personal computer through a communication network. TANIMOTO et al meet limitations of claim 11, including, wherein an image processor to be selected from said plurality of image processors for performing a processing operation at each of said different drawing levels (column 33, lines 51-56- the resolution levels are representative of the drawing levels), however, does not expressly teach a timing applied for performing said processing operation are set in advance to said editing data or as a processing condition. NORTON et al suggest use of the symmetric multiprocessors (SMDs) (column 1, lines 64-67) associated with a host uniprocessor workstation- column 1, lines 10-15 for prediction of parallel processing times between SMDs and a host single processor workstation (column 1, lines 48-55) to suggest "and a timing applied for performing said processing operation are set in advance to said editing data or as a processing condition." It would have been obvious to one skilled in the art at the time of the invention to use the symmetric multiprocessors (SMDs) (column 1, lines 64-67) associated with a host uniprocessor workstation- column 1, lines 10-15 for prediction of parallel processing times between SMDs and a host single processor workstation (column 1, lines 48-55) of NORTON et al to modify a pyramidal processing system facilitating parallel processing of a plurality of

resolution levels to execute local and global o f TANIMOTO et al because both inventions are related to similar technology associated with multiprocessors and a host processor to improve the parallel processing operations of TANIMOTO et al by providing accurate predictions of parallel processing times for accurate prediction of parallel processing times (column 1 of NORTON et al , lines 48-55).

19. As per claim 13, TANIMOTO et al meet limitations of claim 11,

TANIMOTO et al meet limitations of claim 11, including,

wherein an image processor to be selected from said plurality of image processors for performing a processing operation at each of said different drawing levels (column 33, lines 51-56- the resolution levels are representative of the drawing levels), however, does not expressly teach a timing applied for performing said processing operation are set in advance to said editing data or as a processing condition. NORTON et al suggest "and a timing applied for performing said processing operation are set (the at least first conditional is met and underlined) in advance to said editing data (accurate prediction of parallel processing times (column 1 of NORTON et al, lines 48-55) or as a processing condition. "

It would have been obvious to one skilled in the art at the time of the invention to use the symmetric multiprocessors (SMDs) (column 1, lines 64-67) associated with a host uniprocessor workstation- column 1, lines 10-15 for prediction of parallel processing times between SMDs and a host single processor workstation (column 1, lines 48-55) of

NORTON et al to modify a pyramidal processing system facilitating parallel processing of a plurality of resolution levels to execute local and global o f TANIMOTO et al because both inventions are related to similar technology associated with multiprocessors and a host processor to improve the parallel processing operations of TANIMOTO et al by providing accurate predictions of parallel processing times for accurate prediction of parallel processing times (column 1 of NORTON et al , lines 48-55).

20. As per claim 32, TANIMOTO et la as modified meet limitations of claim 7, however, TANIMOTO et al does not expressly teach wherein the different timing represents different processing speeds. NORTON et al, on the other hand teach wherein the different timing represents different processing speeds. It would have been obvious to one skilled in the art at the time of the invention to use the symmetric multiprocessors (SMDs) (column 1, lines 64-67) associated with a host uniprocessor workstation- column 1, lines 10-15 for prediction of parallel processing times between SMDs and a host single processor workstation (column 1, lines 48-55) of NORTON et al to modify a pyramidal processing system facilitating parallel processing of a plurality of resolution levels to execute local and global o f TANIMOTO et al because both inventions are related to similar technology associated with multiprocessors and a host processor to improve the parallel processing operations of TANIMOTO et al by providing accurate predictions of parallel processing times for accurate prediction of parallel processing times (column 1 of NORTON et al , lines 48-55).

21. Claims 12, 27-30 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over TANIMOTO et al, US Patent No. 4,622,632 in view of BUYTAERT et al, US Patent No. 6,041,135.

22. As per claim 12, TANIMOTO et al meet limitations of claim 11, however, does not expressly teach, wherein said plurality of image processors (representative of figure 1, elements 6, 8 and 12) are personal computers.

BUYTAERT et al teach (see figure 1, elements 6-an identification station – column 8, lines 1-8), figure 1, element 8-a preview monitor-column 8, lines 26-28 and figure 1, element 12-a review console-column 8, lines 29-32), wherein said plurality of image processors (representative of figure 1, elements 6, 8 and 12) are personal computers. It would have been obvious to one skilled in the art at the time of the invention to use the means of the three monitors cited above provide users various methods to store image data (i.e., hard disc (column 8, lines 36-42), an optical disc (column 8, lines 43-44 and storage by EEPROM (column 8, lines 54-59) of BUYTAERT et al to modify the pyramidal processing unit of TANIMOTO et al in order to provide a database for storing an optimal processing mode so that the processing may be repeated using the stored processing conditions (column 7, lines 38-42). Therefore, it would have been obvious to modify TANIMOTO et al by BUYTAERT et al.

23. As per claim 27, TANIMOTO et al meet limitations of claim 1, however, does not expressly teach, wherein the higher drawing level is defined by a graphics quality. BUYTAERT et al suggests wherein the higher drawing level is defined by a graphics

quality (column 2, lines 12-16 and column 3, lines 26-35 both discuss high quality images with resolution including a predetermined resolution level used for a preliminary evaluation of the resolution on the monitor screen (column 3, lines 13-17). It would have been obvious to one skilled in the art at the time of the invention to use the determining means for a high quality resolution (column 3, lines 13-35) of BUYTAERT et al to modify the resolution levels and images of the same scene (column 1, line 65-column 2, line 2) of TANIMOTO et al in order to not only provide better image quality for the resolution levels, but, to also reduce computational effort (column 3, lines 26-28). Therefore, it would have been obvious to one skilled in the art to modify TANIMOTO et al with BUYTAERT et al.

24. As per claim 28, TANIMOTO et al as modified meet limitations of claim 27, additionally, TANIMOTO et al teach the following underlined feature among the conditional group of features the image processing method of claim 27, wherein the graphics quality comprises at least one of a resolution (column 33, lines 51-56), number of polygons, raying processing, density scale resolution and an existence/nonexistence of reflected light.

25. As per claim 29, TANIMOTO et al meet limitations of claim 1, however, does not disclose designating image editing data to form the computer graphics image. BUYTAERT et al suggest designating image-editing data to form the computer graphics image

(column 2, lines 25-35 and 59-column 3, line 5 discloses a set of stored parameters are representative of the designated imaging data). It would have been obvious to one skilled in the art at the time of the invention to utilize high image quality processing and diagnostic means (column 3, lines 29-35) of BUYTAERT et al to modify the resolution levels and images of the same scene (column 1, line 65-column 2, line 2) of TANIMOTO et al in order to not only provide better image quality for the resolution levels, but, to also reduce computational effort (column 3, lines 26-28). Further, the addition of BUYTAERT et al "enhances the speed of operation (column 3, lines 32-35). Therefore, it would have been obvious to one skilled in the art to modify TANIMOTO et al with BUYTAERT et al.

26. As per claim 30, TANIMOTO et al as modified meet limitations of claim 27, however, TANIMOTO et al does not expressly teach, wherein the graphics quality is a resolution. BUYTAERT et al suggests wherein the graphics quality is a resolution (column 2, lines 12-16 and column 3, lines 26-35 both discuss high quality images with resolution including a predetermined resolution level used for a preliminary evaluation of the resolution on the monitor screen (column 3, lines 13-17). It would have been obvious to one skilled in the art at the time of the invention to use the determining means for a high quality resolution (column 3, lines 13-35) of BUYTAERT et al to modify the resolution levels and images of the same scene (column 1, line 65-column 2, line 2) of TANIMOTO et al in order to not only provide better image quality for the resolution levels, but, to also reduce computational effort (column 3, lines 26-28).

Therefore, it would have been obvious to one skilled in the art to modify TANIMOTO et al with BUYTAERT et al.

27. As per claim 33, TANIMOTO et al meet limitations of claim 1, including, wherein a plurality of computer graphics algorithms levels are prepared (column 33, lines 51-56-the algorithm levels are representative of the processors at each pyramid processing units level and controlled by figure 2, element 119-the pyramid processing unit controller-column 6, line 35-38), wherein the plurality of drawing levels are prepared for each of the plurality of computer graphics algorithms (column 33, lines 51-56-the algorithm levels are representative of the processors at each pyramid processing units level and controlled by figure 2, element 119-the pyramid processing unit controller-column 6, line 35-38), and wherein the drawing levels are based on a display resolution (column 33, lines 51-56), however, does not disclose stored in a database on a personal computer. BUYTAERT et al suggest storing in a database on a personal computer (and provides a database for storing an optimal processing mode so that the processing may be repeated using the stored processing conditions (column 7, lines 38-42).

It would have been obvious to one skilled in the art at the time of the invention to use the means of the three monitors cited above provide users various methods to store image data (i.e., hard disc (column 8, lines 36-42), an optical disc (column 8, lines 43-44 and storage by EEPROM (column 8, lines 54-59) of BUYTAERT et al to modify the pyramidal processing unit of TANIMOTO et al in order to provide a database for storing

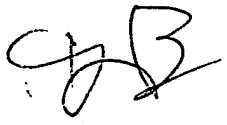
an optimal processing mode so that the processing may be repeated using the stored processing conditions (column 7, lines 38-42). Therefore, it would have been obvious to modify TANIMOTO et al by BUYTAERT et al.

Conclusion

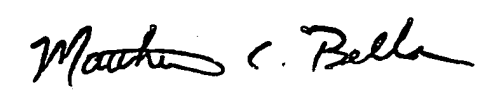
Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANTHONY J BLACKMAN whose telephone number is 703-305-0833. The examiner can normally be reached on FLEX SCHEDULE.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MATTHEW BELLA can be reached on 703-308-6829. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



ANTHONY J BLACKMAN
Examiner
Art Unit 2676



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